Remarks/Arguments:

Applicants thank the Examiner for the Interview with him on April 26, 2004, and for his helpful suggestions in amending the claims.

Applicants have now cancelled claims 1, 5, 6 and 7. Dependent claims 2-4 and 8 have been amended to depend from claim 20.

Section 102/103 Rejections:

Independent claims 9, 14 and 20 have been rejected as being anticipated by Anderson. Applicants respectfully submit that this rejection is overcome for the reasons set forth below.

Amended claim 9 now includes features which are not suggested by the cited reference, namely:

- **a register and an edge detector both coupled between the first and second processors** (newly added),
- the edge detector coupled to the register for detecting active logic levels stored in the register and **converting each active logic level into an interrupt signal**, and
- at least one line coupled between the edge detector and an interrupt terminal of the second processor for **routing one of the interrupt signals to the interrupt terminal.**

Basis for amended claim 9 may be seen, for example, in FIG. 4. As shown, register 44 and edge detector 45 are **both coupled between first processor 41 and second processor 46**. Register 44 receives the data on data bus 81 from first processor 41, and provides an active logic level for each data bit that is a "1", for example. Each of these active logic level data bits ("1s", for example) are then converted into active logic level signals, which become interrupt signals that are routed to interrupt terminals of the second processor.

In this manner, the invention uses active bits from a single data word (placed by a first processor onto a data bus) as interrupt signals that may be routed to interrupt terminals of a second processor. This advantageously reduces the number of dedicated output terminals required in the first processor, because the need for dedicated interrupt signal outputs are eliminated.

Anderson discloses a method for synchronizing a first set of frames corresponding to a first processor with a second set of frames corresponding to a second processor. Based on a value stored in a register, the frame length of the first set of frames is adjusted to be synchronized with the second set of frames. Anderson, however, does **not** disclose the features of amended claim 9. Anderson does **not** disclose **a register and an edge detector both coupled between the first and second processors**. Anderson does **not** disclose (1) **an edge detector coupled to the register for detecting active logic levels stored in the register** and (2) **converting each active logic level into an interrupt signal**. Furthermore, Anderson does **not** disclose **a line coupled between the edge detector and the interrupt terminal of the second processor for routing the interrupt signal to an interrupt terminal of the second processor**.

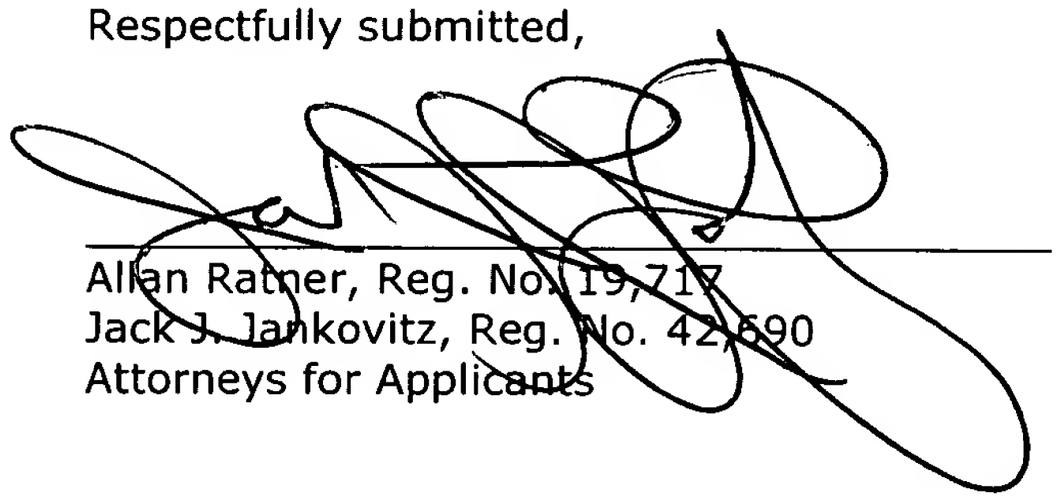
Favorable reconsideration is requested for amended claim 9. Although not the same, claims 14 and 20 have been amended to include features similar to amended claim 9. Amended claims 14 and 20 are not subject to rejection in view of the cited references for the same reasons set forth for amended claim 9.

Dependent claims 10-13 depend from claim 9. Dependent claims 15-19 depend from claim 14. Dependent claims 21-26, 2-4 and 8 depend from claim 20. These dependent claims are, therefore, not subject to rejection in view of the cited references for at least the same reasons set forth for amended claim 9. Favorable reconsideration is respectfully requested.

Conclusion

Claims 2-4 and 8-26 are in condition for allowance.

Respectfully submitted,



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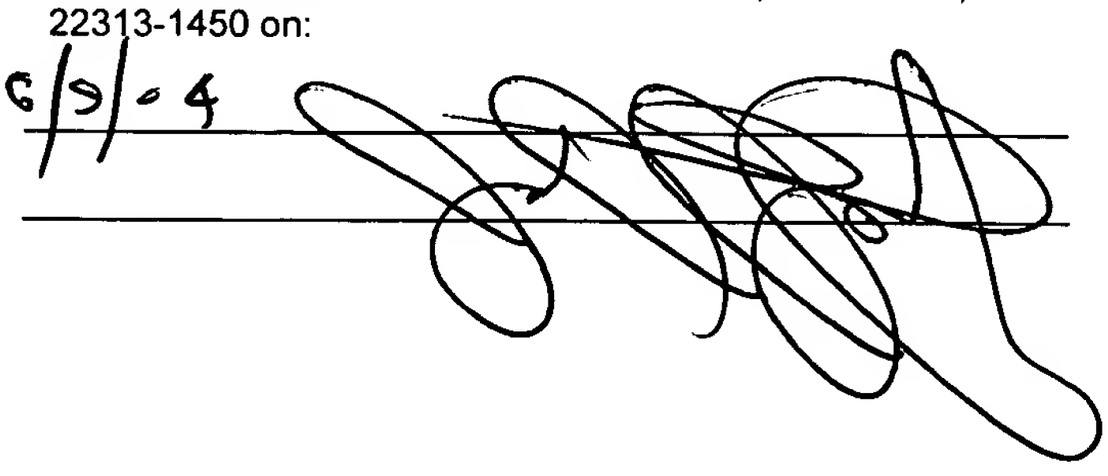

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